```
   14       JTEMP = IPS(K)
            IPS(K) = IPS(IDXPIV)
            IPS(IDXPIV) = JTEMP
   15    KP = IPS(K)
         PIVOT = UL(KP,K)
CPL2  RECIP=1.0/UL(KP,K)
         KP1 = K+1

         DO 16 I = KP1,N
            IP = IPS(I)
CPL1  IF(UL(IP,K) .EQ. 0.0) GO TO 16
            EM = -UL(IP,K)/PIVOT
CPL2  EM=-UL(IP,K)*RECIP
            UL(IP,K) = -EM
            DO 16 J = KP1,N
CPL1  IF(UL(KP,J) .EQ. 0.0) GO TO 16
               UL(IP,J) = UL(IP,J) + EM*UL(KP,J)
C           INNER LOOP.  USE MACHINE LANGUAGE CODING IF COMPILER
C           DOES NOT PRODUCE EFFICIENT CODE.
   16    CONTINUE
   17 CONTINUE
      KP = IPS(N)
      IF (UL(KP,N)) 19,18,19
   18 CALL SING(2)
   19 RETURN
      END
      SUBROUTINE SOLVE (NN, NMAX, UL, B, X, IPS)
      DIMENSION UL(NMAX,NMAX),B(NMAX),X(NMAX),IPS(NMAX)
      N = NN
      NP1 = N+1
C
      IP = IPS(1)
      X(1) = B(IP)
      DO 2 I = 2,N
         IP = IPS(I)
         IM1 = I-1
         SUM = 0.0
         DO 1 J = 1,IM1
CPL4  IF(UL(IP,J) .EQ. 0.0) GO TO 1
CPL5  IF(X(J) .EQ. 0.0) GO TO 1
            SUM = SUM + UL(IP,J)*X(J)
    1 CONTINUE
    2 X(I) = B(IP) - SUM
C
      IP = IPS(N)
      X(N) = X(N)/UL(IP,N)
      DO 4 IBACK = 2,N
      I = NP1-IBACK
C        I GOES (N-1),...,1
         IP = IPS(I)
         IP1 = I+1
         SUM= 0.0
         DO 3 J = IP1,N
CPL6  IF(UL(IP,J) .EQ. 0.0) GO TO 3
CPL7  IF(X(J) .EQ. 0.0) GO TO 3
            SUM = SUM + UL(IP,J)*X(J)
    3 CONTINUE
    4 X(I) = (X(I)-SUM)/UL(IP,I)
      RETURN
      END
```


References

FORSYTHE, GEORGE E., and MOLER, CLEVE B. (1967). *Computer Solution of Linear Algebraic Systems*, Prentice-Hall Inc., Englewood Cliffs, New Jersey.

SHERMAN, ANDREW H. (1975). *Yale Sparse Matrix Package User's Guide*, Lawrence Livermore Laboratories Document UCID-30114, Livermore, California.

Book reviews

Rational Fault Analysis, edited by R. Saeks and S. R. Liberty, 1977; 256 pages. (*Marcel Dekker*, S FR 91)

This book is the result of a symposium held in August 1977 at Texas Technical University. The individual papers cover methods of fault location and prevention in digital systems, although some papers deal with analogue systems.

There are two extensive bibliographies, one dealing with analogue systems and the other with digital systems. These have 193 and 1180 references respectively and together are one third of the book. The first two papers give details of methods of fault analysis using graph theory and prove some underlying theorems. The next paper gives some design guides for making sequential systems fault tolerant and making fault location easy. The next paper considers the online detection and location of faults in linear analogue systems.

A paper on modelling faults follows and this deals with the types of fault model which are used in analysis and the generation of test sets. Computer aided fault analysis is next surveyed and hints are given for designers to incorporate features to make testing easier. The 'reliable design of software' is the next topic and this gives some hints of how to attain a sufficiently reliable design.

Next is a further theoretical paper followed by one on fault prediction which deals with component life, fault detection and replacement. The final paper is concerned with fault finding in lumped parameter networks.

This is a rather specialised book but is essentially unique in its coverage. It is recommended reading for those designing large modern electronic systems.

D. J. WHEELER (Cambridge)

Analysis and Design of Sequential Digital Systems, by L. F. Lind and J. C. C. Nelson, 1977; 146 pages. (*Macmillan*, £8·95 hard cover, £4·50 paper)

The text is aimed at final year undergraduates and practising engineers and adequately covers the operation of synchronous and asynchronous sequential logic systems. Liberal use is made of Karnough maps, state tables, timing waveforms and other design aids with due attention to hazard and race conditions. Several small examples are given and discussed at length.

Although the intending logic designer will be better equipped with design techniques, having read the 150 or so pages of this book, it is regrettable that certain related matters are given scant or no attention. The analogue nature of logic circuits is completely ignored—all waveforms having wonderfully square corners. No space is given to current technology or its packaging, nor to programmed logic arrays or read only memories. One would have thought that if this book is aimed at the practising engineer then these matters would be of some consequence. It would also have been useful to see at least one substantial design to illustrate how the sometimes involved proposed design techniques stand up when more than three flipflops are involved.

The book is for the most part readable though restricted in scope. Adequate references are given to other related works at the end of each chapter but an intending reader may find a practical design course with MSI logic a useful adjunct.

P. M. HAINE (Rugby)

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