the buffer allocation per call in each node will be progressively increased from an initial value of one up to a preset limit in each node as successive packets of the call are handled; onset of congestion produces a progressive decrease of buffer allocation down to a minimum of one buffer per extant virtual call in each node.

The system outlined proved to behave badly in the face of a heavy applied load, throughput falling to a value much below the optimum, though lockup was still avoided. It was deduced that more efficient congestion control was required. This was provided by limiting the number of buffers available from the node pool for incoming traffic from outside the net. A series of experiments addressed the question of performance with various buffer pool sizes and input buffer limits; the relationship is complex, but it seems that optimum performance is obtained with an input buffer limit of about three buffers and a total buffer pool size per node of about 16 buffers.

This technique of efficient throttling of incoming traffic according to buffer pool occupancy has much in common with the techniques used in the NPL experiments.

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Book reviews

Digital Computer Circuits and Concepts, 2nd edition, by B. Deem, K. Muchow and A. Zeppa, 1977; 487 pages. (*Prentice Hall*, £12·80 paper, £20·35)

Authors who wrote books on hardware about five or six years ago were in a particularly unfortunate position of seeing microprocessors and other large scale integrated circuit techniques burst on the scene just as their books appeared on library shelves with no mention of such devices. This required rapid second editions. Although the Deem, Muchow and Zeppa text falls into this category, it is a particularly successful member of its genre. The last three chapters and appendices, thoroughly and fully explore up-to-date concepts in LSI memories and microprocessors.

The rest of the text proceeds in a classical way: number systems, binary arithmetic, then on to Boolean synthesis techniques. After dismissing combinational synthesis in a dozen or so pages, the book talks of simple circuits (gates, flip flops) and subsystems (registers and counters). There is no attempt whatsoever to introduce the reader to any formalism in the design of sequential systems or to important issues such as hazards and the testing of systems. This makes the book clearly unsuitable for courses where one tries to convey a grasp of the fundamental principles underlying digital systems, leaving it in the realm of courses intended to train technicians rather than design engineers. Perhaps this is what is meant by the blurb on the jacket, which states that the book was written to '. . . integrate academic theoretical instruction with current industrial practices . . .'. The integration, however, seems to have been achieved by ignoring the first of the two items altogether.

I. ALEKSANDER (Uxbridge)

Digital Signal Processing, by A. Peled and B. Liu, 1976; 304 pages. (*John Wiley*, £10·50)

This is an excellent text book for a rapidly expanding field. Peled and Liu have considerably updated previous standard works on the subject, principally by describing not only the mathematical foundations of the processes involved but also the implementation of such techniques using PL/1 computer programs and circuits of dedicated hardware systems as well. There is a good introduction to the theory of filtering followed by chapters on the design of digital filters and their use.

Digital filtering is now dominated by the availability of the Fast Fourier Transform and this topic is covered in depth with several examples of both software and hardware FFT processors. Unfortunately this book does not cover the design of filters using microprocessors; it is to be hoped that a second edition may remedy this.

A. M. CRUISE (Dorking)