Minimising the NAND-NOR-XOR network of modulo 2 sum of boolean products

Z. M. Lotfi and A. J. Tosser

Université de Nancy I, Laboratoire d'Electronique CO 140, 54037 Nancy Cedex, France

Properties of the exclusive-OR (XOR) gate are used in order to determine the minimum realisation cost of logical functions written as a modulo 2 sum of minterms (factorised or not). Saving of NAND and NOR gates are tabulated. Extended results about opportune type of factoring are thus known.

Les propriétés de l'opérateur OU-exclusif permettent de déterminer le coût minimal de réalisation de fonctions logiques écrites sous forme d'une somme modulo 2 de mintermes (factorisés ou non). Les nombres de portes NAND et NOR économisées sont tabulés et fournissent des renseignements étendus sur le type de factorisation qu'il est opportun de réaliser.

(Received September 1977)

1. Introduction

Several papers have been published about the implementation of XOR gates in AND-OR networks (Miessler, 1972; Csanky, 1969; Edwards, 1975; Mukhopadhyay and Schmitz, 1970; Bivol, 1968; Schmookler, 1969; Banks and Majithia, 1973; Edwards and Hurst, 1976) or in NAND-NOR networks. More recently it has been proposed to build universal module with the aid of XOR gates.

The purpose of this paper is to examine the opportunity of introducing XOR gates in a modulo 2 sum of minterms in order to minimise the (NAND-NOR) XOR networks built in NAND and NOR gates, when the output gate is a XOR gate. This question is even of interest in biomedical engineering, since restrictions in power dissipation and propagation delay time are not always consistent with the implementation of LSI devices. For this purpose some typical properties of the XOR operator are used.

2. Some properties of the XOR operator

2.1. *Symmetry property*

The symmetry property of the XOR operator is defined as

$$a \oplus b = \bar{a} \oplus \bar{b}$$

Hence

$$ab \oplus cd = \overline{ab} \oplus \overline{cd} = (a/b) \oplus (c/d) \quad (1)$$

2.2. *Negation property*

It is true that

$$\overline{a \oplus b} = \bar{a} \oplus b = a \oplus \bar{b}$$

Hence

$$a \oplus bc = \overline{a \oplus \overline{bc}}$$

$$a \oplus bc = \overline{a \oplus (b/c)} \quad (2)$$

Similarly

$$\bar{a} \oplus bc = a \oplus \overline{bc} = a \oplus (b/c) \quad (3)$$

$$ab \oplus cd \oplus ef = \overline{ab} \oplus \overline{cd} \oplus \overline{\overline{ef}} = (a/b) \oplus (c/d) \oplus (\overline{e/f})$$

and, more generally,

$$\underbrace{ab \oplus \ldots \oplus yz}_{D \text{ terms}} = (a/b) \oplus \ldots \oplus (y/z) \quad (4)$$

$D = 2D'$ terms

$D = 2\,D'$

$$\underbrace{ab \oplus \ldots \oplus xy}_{D \text{ terms}} = (a/b) \oplus \ldots \oplus \overline{(x/y)} \text{ one overlining}$$

$D = 2\,D' + 1$ $\quad D = (2D' + 1)$ terms $\quad (5)$

whereas

$$\bar{a}\bar{b} \oplus \ldots \oplus \bar{y}\bar{z} = (a \downarrow b) \oplus \ldots \oplus (y \downarrow z) \quad (6)$$

hence

$$\underbrace{\bar{a} \oplus \bar{b} \oplus \ldots \oplus \bar{z}}_{c \text{ terms}} = a \oplus b \oplus \ldots \oplus z \quad (7)$$

$c = 2\,c'$

$$\underbrace{\bar{a} \oplus \bar{b} \oplus \ldots \oplus \bar{y}}_{c \text{ terms}} = a \oplus b \oplus \ldots \oplus x \oplus \bar{y} \text{ one overlining} \quad (8)$$

$c = 2\,c' + 1$

Another transformation gives

$$abc\bar{d} \oplus efg\bar{h} = \overline{\overline{abc}\,\bar{d}} \oplus \overline{\overline{efg}\,\bar{h}} = ((a/b) \downarrow c \downarrow d) \oplus ((e/f) \downarrow g \downarrow h)$$

and more generally

$$\underbrace{abc\bar{d} \oplus \ldots \oplus wxy\bar{z}}_{M \text{ terms}} = \underbrace{((a/b) \downarrow c \downarrow d) \oplus \ldots \oplus ((w/x) \downarrow y \downarrow z)}_{M \text{ terms}} \quad (9)$$

A special feature is

$$ab\bar{c} \oplus efg = \overline{\overline{ab}\,\bar{c}} \oplus \overline{\overline{efg}} = \overline{ab\bar{c}} \oplus \overline{efg} = ((a/b) \downarrow c) \oplus (e/f) \downarrow g) = (a/b/\bar{c}) \oplus (e/f/\bar{g})$$

and more generally

$$\underbrace{ab\bar{c} \oplus \ldots \oplus xy\bar{z}}_{M = 2M'} = ((a/b) \downarrow c) \oplus \ldots \oplus ((x/y) \downarrow z) = (a/b/\bar{c}) \oplus \ldots \oplus (x/y/\bar{z}) \quad (10)$$

also

$$\underbrace{a\bar{b}\bar{c} \oplus \ldots \oplus x\bar{y}\bar{z}}_{M} = (\bar{a} \downarrow b \downarrow c) \oplus \ldots \oplus (\bar{x} \downarrow y \downarrow z) \quad (11)$$

A special case is

$$ab \oplus c \oplus d = \overline{\overline{ab}} \oplus c \oplus d = (\overline{a/b}) \oplus c \oplus d \quad (12)$$

Another case is

$$ab \oplus cd \oplus e \oplus f = \overline{ab} \oplus \overline{cd} \oplus e \oplus f = (a/b) \oplus (c/d) \oplus e \oplus f \quad (13)$$

3. Minimum (NAND-NOR) XOR synthesis of sum of minterms

Five types of minterms have been defined in previous papers (Tosser and Brochet, 1974; Tosser, 1976; 1975): we respectively defined the indexed minterms m_D, m_C, and m_M as direct, complemented and mixed minterm (product of binary variables) i.e.

$$m_D = \prod_i x_i,\ m_C = \prod_j \bar{x}_j,\ m_M = \prod_i x_i \cdot \prod_j \bar{x}_j \text{ with } i \neq j$$

where x_i and x_j are binary variables; x_i and $\bar{x}_i$ are called first order direct and first order complemented minterms, respectively. D, d, C, c, and M are respectively the number of direct, first order direct, complemented, first order complemented and mixed minterms constituting the modulo 2 sum of minterms.

From the above relations a complete tabulation of the (NAND-NOR) XOR realisation of the 31 possible sets of type of modulo 2 sum of typical minterms is given (**Table 1**).

The realisation cost of the first five sums of typical minterms are deduced from the results of the above paragraph; line 1 of Table 1 is derived from relations 4 and 5; line 2 is obvious; line 3 comes from relation 6; line 4 comes from relations 7 and 8; line 5 comes from relations 9, 10 and 11. The other possible sets of sums are obtained from suitable combinations of typical minterms and their realisation costs are deduced from the first five realisation costs, taking into account some further allowed saving of gates: for instance, the realisation cost of the sum of first order complemented and mixed minterms (line 9) is M NAND- and M NOR-gates, whereas the separate realisation costs respectively are 0 or 1 inverter gate (if c is even or odd) (line 4) and M NAND and M NOR gate (line 5); one gate is saved by simultaneous realisation since

$$\underbrace{\bar{a} \oplus \ldots \oplus \bar{u}}_{c \text{ terms}} \oplus \alpha\beta\bar{\gamma}\bar{\delta} \oplus \ldots = a \oplus \ldots \oplus u \oplus \alpha\beta\overline{\bar{\gamma}\bar{\delta}} \oplus \ldots = a \oplus \ldots \oplus u \oplus (\alpha/\beta/(\gamma\downarrow\delta)) \oplus$$

$c = 2c' + 1$

and

$$\bar{a} \oplus \ldots \oplus \bar{t} \oplus \alpha\beta\bar{\gamma}\bar{\delta} \oplus \ldots = a \oplus \ldots \oplus t \oplus \overline{\alpha\beta}\bar{\gamma}\bar{\delta} \oplus \ldots = a \oplus \ldots \oplus t \oplus ((\alpha/\beta)\downarrow\gamma\downarrow\delta) \oplus \ldots$$

$c = 2c'$

Comparing equation (10), or (11), with equation (9) justifies special cases **, or *.

For case number 12, when D and C are both even or odd, i.e. $(D + c)$ is even, the total number of overlinings is zero, whereas an overlining remains when $(D + c)$ is odd. It is the same situation that occurs in cases 19 and 30.

4. Factoring within a modulo 2 sum of minterms

When a minterm or a binary variable is common to several terms of a modulo 2 sum of minterms, the distributivity of the AND operator and the symmetry of the exclusive-OR (XOR) operator allows typical transformations of the binary addition in the general factorised form as follows:

$$\ldots \oplus (m_1 \,.\, m_3) \oplus (m_1 \,.\, m_4) = \ldots \oplus (m_1\,(m_3 \oplus m_4))$$

where m_1 is the *common minterm*, m_3 and m_4 are the *factorised minterms*. General results about the realisation cost of factorised modulo 2 sum of direct, complemented, mixed, mixed and direct, mixed and complemented minterms have been previously presented (Lotfi, 1977). They are calculated in an algebraic way; for instance, when the initial minterms are direct minterms and when the common minterm is direct and the factorised minterms are direct and first order direct minterms, the factorised expression is transformed as follows:

$$\ldots \oplus \prod_i x_i \Big(\sum_{k=1}^{D} \prod_j^k x_j \oplus \sum_{l=1}^{d} x_l\Big) = \ldots \oplus \overline{\prod_i x_i \Big(\sum_k \prod_j x_j \oplus \sum_l x_l\Big)}$$

the symbol $\sum$ representing a modulo 2 sum,
Hence

$$\ldots \oplus \prod_i x_i \Big(\sum_k \prod_d^k x_d \oplus \sum_l x_l\Big)$$

$$= \ldots \oplus \Big(\overline{\ldots/x_i/\ldots/(\ldots \oplus (\ldots/x_j/\ldots) \oplus \ldots \oplus x_l \oplus \ldots)}\Big)$$

if D is even (14)

$$= \ldots \oplus (\ldots/x_i/\ldots/(\ldots \oplus \overline{(\ldots/x_j/\ldots)} \oplus \ldots \oplus x_l \oplus \ldots))$$

if D is odd

Another solution would be

$$\ldots \oplus \prod_i x_i \Big(\sum_k \prod_j^k x_j \oplus \sum_l x_l\Big) = \ldots \oplus \overline{\prod_i x_i \Big(\sum_k \prod_j^k x_j \oplus \sum_l x_l\Big)}$$

$$= \ldots \oplus ((\ldots/x_i/\ldots)\downarrow((\ldots \oplus \overline{(\ldots/x_j/\ldots)} \oplus \ldots \oplus x_l \oplus \ldots))$$

if D is even

$$= \ldots \oplus ((\ldots/x_i/\ldots)\downarrow((\ldots \oplus (\ldots/x_j/\ldots) \oplus \ldots \oplus x_l \oplus \ldots))$$

if D is odd (15)

The lower realisation cost when D is even ($D = 2\,D'$) corresponds to the first development; 1 XOR, (D + 1) NAND and 1 INV gates are used.

The lower realisation cost when D is odd ($D = 2\,D' + 1$) corresponds to the second development; 1 XOR, (D + 1) NAND, 1 NOR gates are used. If the modulo 2 sum of minterms S contains an even number of direct minterm, the total expression could be written as

$$S = \prod_t x_t \oplus \prod_u x_u \oplus \prod_v x_v \oplus \prod_i x_i \Big(\sum_{k=1}^{2D'} \prod_j^k x_j \oplus \sum_{l=1}^{d} x_l\Big)$$

and transformed in

$$S = (\ldots/x_t/\ldots) \oplus (\ldots/x_u/\ldots) \oplus \overline{(\ldots/x_v/\ldots) \oplus (\ldots/x_i/\ldots/(\ldots \oplus (\ldots/x_j/\ldots) \oplus \ldots \oplus x_1 \oplus \ldots))}$$

and after reduction of this overlining

$$S = (\ldots/x_t/\ldots) \oplus (\ldots/x_u/\ldots) \oplus (\ldots/x_v\ldots) \oplus (\ldots/x_i/\ldots/(\ldots \oplus (\ldots/x_j/\ldots \oplus \ldots \oplus x_1 \oplus \ldots)) \quad (16)$$

It appears that the inverter gate realising the factorised sum merges with the inverter gate realising an unfactorised minterm, which is exactly the footnote * in **Table 2**. The minimum synthesis cost is obtained in this way for any typical common minterm and typical sum of factorised minterms, and detailed tabulations are drawn (Lotfi, 1977). Hence, the saving of gates is calculated from the general (NAND-NOR) XOR synthesis cost of modulo 2 sum given in Table 1 (the cases * and ** are not considered) and from the minimum synthesis cost of the factorised expression.

The extended tabulation of the saving of gates can be shortened since it is noted that *no saving of gates is obtained when the initial minterms become factorised minterms of the same type*. A thorough algebraic study of the expression of the saving of gates shows (Tosser and Lotfi, 1978) that a further reduction of the tabulation is obtained if some simple saving conditions are introduced. For instance the factorised realisation cost of $(D + d)$ direct minterms, when a direct common minterm exists, is 1 ⊕ , $(D + 1)$/ and 1 INV if D is even and 1 ⊕ , $(D + 1)$/ and 1↓ if D is odd. (equations (14) and (15)) whereas the unfactorised realisation needs $(D + d)$/ if D is even and $(D + d)$/ and 1 INV if D is odd. Hence the gate saving is:

$$D + d - (D + 3) = d - 3 \text{ if } D \text{ is even,}$$

$$D + d + 1 - (D + 3) = d - 2 \text{ if } D \text{ is odd.}$$

But when D is even the INV gate may reduce with another INV gate related to unfactorised minterms, as shown in equation (16). Hence the number of saved gates is marked $d - 3$* on Table 2. The saving conditions are D is even (or odd) and $d \neq 0$ because no saving is obtained if both common and factorised minterms are of the same type. All the data about saving of gates are thus introduced in Table 2; the special

Table 1 (NAND-NOR) XOR minimum synthesis. Number of NAND, NOR and INVERTER gates needed in addition to the output XOR gate.

	Type of m_i	*Number of minterms*	*Number of gates* /	↓	∅	*Comments*
1	Direct	D	D	0	0	When D is even
			D	0	1	odd
2	1st order direct	d	0	0	0	
3	Complemented	C	0	C	0	
4	1st order complemented	c	0	0	0	When c is even
			0	0	1	odd
5	Mixed	M	M*	M**	0	
6	Direct and mixed	$D + M$	$D + M$*	M**	0	
7	1st direct and mixed	$d + M$	M*	M**	0	
8	Complemented and mixed	$C + M$	M*	$C + M$**	0	
9	1st complemented and mixed	$c + M$	M*	M**	0	
10	Direct and 1st order direct	$D + d$	D	0	0	When D is even
			D	0	1	odd
11	Direct and complemented	$D + C$	D	C	0	When D is even
			D	C	1	odd
12	Direct and 1st order complemented	$D + c$	D	0	0	When $D + c$ is even
			D	0	1	odd
13	1st order direct and complemented	$d + C$	0	C	0	
14	1st order direct and 1st order complemented	$d + c$	0	0	0	When c is even
			0	0	1	odd
15	Complemented and 1st order complemented	$C + c$	0	C	0	When c is even
			0	C	1	odd
16	Direct, 1st order direct and complemented	$D + d + C$	D	C	0	When D is even
			D	C	1	odd
17	Direct, 1st order direct and 1st order complemented	$D + d + c$	D	0	0	When $D + c$ is even
			D	0	1	odd
18	Direct, 1st order direct and mixed	$D + d + M$	$D + M$*	M**	0	
19	Direct, complemented and 1st order complemented	$D + C + c$	D	C	0	When $D + c$ is even
			D	C	1	odd
20	Direct, complemented and mixed	$D + C + M$	$D + M$*	$C + M$**	0	
21	Direct, 1st order complemented and mixed	$D + c + M$	$D + M$*	M**	0	
22	1st order direct, complemented and 1st order complemented	$d + C + c$	0	C	0	When c is even
			0	C	1	odd
23	1st order direct, complemented and mixed	$d + C + M$	M*	$C + M$**	0	
24	1st order direct, 1st order complemented and mixed	$d + c + M$	M*	M*	0	
25	Complemented, 1st order complemented and mixed	$C + c + M$	M*	$C + M$**	0	
26	Direct, 1st order direct, complemented and mixed	$D + d + C + M$	$D + M$*	$C + M$**	0	
27	Direct, 1st order direct, 1st order complemented and mixed	$D + d + c + M$	$D + M$*	M**	0	
28	Direct, complemented, 1st order complemented and mixed	$D + C + c + M$	$D + M$*	$C + M$**	0	
29	1st order direct, complemented, 1st order complemented and mixed	$d + C + c + M$	M*	$C + M$**	0	
30	Direct, 1st order direct, complemented, 1st order complemented	$D + d + C + c$	D	C	0	When $D + c$ is even
			D	C	1	odd
31	1st order direct, complemented, 1st order complemented and mixed	$D + d + C + c + M$	$D + M$*	$C + M$**	0	

Notes
/ is the symbol of NAND gate
↓ is the symbol of NOR gate
∅ is the symbol of inverter gate
*When a mixed minterm contains only one true variable an INV gate may be substituted for a NAND gate; several INV gates related to the same variable may then be replaced by one gate.
**When an even number of mixed minterms contain only one inverted variable an INV gate may be substituted for a NOR gate; several INV gates related to the same variable may then be replaced by one gate.

cases *, ** and † are then examined whenever they occur; these situations must not be forgotten especially when practical factorisation is used.

5. Practical application

We now consider some examples.

Table 2 Saving of gates by factorisation

Line	Type of initial minterms	Type of common minterm	Number of factorised minterms	Number of saved NAND-NOR-gates	Saving conditions
	direct	direct or			
1		1st order direct	$D + d$	$d - 3$*	D is even } and $d \neq 0$
2			$D + d$	$d - 2$	D is odd }
3			d	$d - 3$*	d is even
4			d	$d - 2$	d is odd
5	complemented	complemented or 1st order	$C + c$	$c - 3$	c is even
		or			
6		complemented	c	$c - 2$	c is odd
7	mixed	direct or 1st order direct	$C + c + M$	$C + 2c - 3$*	C or $c \neq 0$
8		complemented or 1st order	$D + d + M$	$D + 2d - 2$	D is odd or $M \neq 0$
9		complemented		$D + 2d - 3$	D is even and D or $d \neq 0$
10		mixed	$D + d + C + c + M$	$D + 2d + C + 2c - 3$	D or d or C or $c \neq 0$
11	direct and mixed	direct or 1st order direct	$D + d + C + c + M$	$d + C + 2c - 3$*	d or C or $c \neq 0$
12	complemented	complemented or 1st	$D + d + C + c + M$	$D + 2d + c - 3$	$D + c$ is even } and $D \neq 0$
13	and mixed	order complemented		$D + 2d + c - 2$	$D + c$ is odd or $M \neq 0$ } or $d \neq 0$ or $c \neq 0$

Comments
D, d, C, c, M is respectively the number of direct, 1st order direct, complemented, 1st order complemented and mixed minterms.
*an inverter-gate may reduce with another inverter-gate related to unfactorised minterms

5.1. *1st example: a Reed-Muller expanded form*
The function has been proposed by Mukhopadhyay and Schmitz (1970)

$$f = \bar{x}_3 \oplus \bar{x}_2\,\bar{x}_3 \oplus x_1\,\bar{x}_2\,x_5 \oplus \bar{x}_3\,\bar{x}_4\,x_5 \oplus x_1\,\bar{x}_2\,\bar{x}_3\,\bar{x}_4 \oplus x_1\,\bar{x}_2\,\bar{x}_4\,x_5 \oplus \bar{x}_2\,\bar{x}_3\,\bar{x}_4\,x_5$$

The factoring possibilities are given in **Table 3**.

Table 3

Number and type of initial minterms	common minterm	Factorised minterms	saving of gates	comments
3, mixed	x_1	$C = 1$, $M = 2$	NO*	Table 2 line 7
1, complemented	$\bar{x}_2$	$D = 1$,	NO	Table 2
4, mixed		$c = 1$, $M = 3$		line 12
1, complemented	$\bar{x}_3$	$c = 1$,	NO	Table 2
3, mixed		$M = 3$		line 13
4, mixed	$\bar{x}_4$	$M = 4$	NEVER	
4, mixed	x_5	$C = 2$, $M = 2$	NO*	Table 2 line 7

*an equivalent solution is obtained by substituting x_3 for $\bar{x}_3$ and inverting the factorised term.

5.2. *2nd example*
The function to be minimised is

$$f = x_1\,\bar{x}_3 \oplus x_2\,\bar{x}_3 \oplus \bar{x}_2\,\bar{x}_3\,\bar{x}_4\,\bar{x}_5 \oplus x_2\,\bar{x}_3\,x_4\,x_5 \oplus x_3\,\bar{x}_4 \oplus x_2\,x_3\,x_4 \oplus x_1\,x_3\,x_4\,x_5 \oplus \bar{x}_1\,\bar{x}_2\,\bar{x}_3$$

This modulo 2 sum contains $M = 5$ mixed minterms, $D = 2$ direct minterms and $C = 1$ complemented minterm; the (NAND—NOR) XOR minimum synthesis generally requires (Table 1, line 20) $D + M^* = 7^*$ NAND gates, $C + M^{**} = 6^{**}$ NOR gates and 1 XOR gate, i.e. a total number of 14 gates. But 7*/ reduces to 3 / and 4 ∅ since four mixed minterms contain a true state of only one variable; 4 ∅ reduces to 3 ∅ since two minterms, i.e. $x_3\,\bar{x}_4$ and $\bar{x}_1\,\bar{x}_2\,x_3$, contain the one true state x_3. the corresponding (NAND-NOR) XOR expression of f is:

$$f = (\underset{2}{\bar{x}_1} \downarrow \underset{3}{x_3}) \oplus (\underset{1}{\bar{x}_2} \downarrow \underset{4}{x_3}) \oplus (\underset{6}{x_2} \downarrow x_3 \downarrow x_4 \downarrow x_5) \oplus (\underset{7}{x_3} \downarrow \underset{8}{(x_2/x_4/x_5)}) \oplus (\underset{9}{\bar{x}_3} \downarrow \underset{10}{x_4}) \oplus \underset{11}{(x_2/x_3/x_4)} \oplus \underset{12}{(x_1/x_3/x_4/x_5)} \oplus \underset{13}{(x_1 \downarrow x_2 \downarrow \bar{x}_3)}$$

for which 13 gates are required. (3/, 6↓, 3 ∅, 1 ⊕).

But 6**↓ may be 4 ↓ and 2 ∅ since an even number of mixed minterms, i.e. $x_1\,\bar{x}_3$ and $x_2\,\bar{x}_3$ for instance contain one inverted variable; 2 ∅ reduced to 1 ∅ since it is the same variable. Then 7*/ reduces to 5 / and 2 ∅, since two mixed minterms (omitting $x_1\,\bar{x}_3$ and $x_2\,\bar{x}_3$) contain only one true variable. And 2 ∅ reduces to 1 ∅ since the inversion of x_3 has already been realised at the previous step. The (NAND-NOR) XOR expression of f is

$$f = \underset{2}{(x_1/\bar{x}_3)} \oplus \underset{1}{(x_2/\bar{x}_3)} \oplus (\underset{5}{x_2} \downarrow x_3 \downarrow x_4 \downarrow x_5) \oplus (\underset{6}{x_3} \downarrow \underset{7}{(x_2/x_4/x_5)}) \oplus (\underset{8}{\bar{x}_3} \downarrow x_4) \oplus \underset{9}{(x_2/x_3/x_4)} \oplus \underset{10}{(x_1/x_3/x_4/x_5)} / \oplus \underset{11}{(x_1 \downarrow x_2 \downarrow \bar{x}_3)}$$

for which 11 gates are required (5/, 4↓, 1 ∅, 1 ⊕). It is the minimum (NAND-NOR) XOR synthesis of this modulo 2 sum of minterms using the special cases * and ** given in Table 1. Other savings of gates could be obtained from the following transformations.

The first 4 terms may be written

$$x_1\,\bar{x}_3 \oplus x_2\,\bar{x}_3 \oplus \bar{x}_2\,\bar{x}_3\,\bar{x}_4\,\bar{x}_5 \oplus x_2\,\bar{x}_3\,x_4\,x_5 = \bar{x}_3\,(x_1 \oplus x_2 \oplus \bar{x}_2\,\bar{x}_4\,\bar{x}_5 \oplus x_2\,x_4\,x_5)$$

The initial mixed and complemented minterms are factorised; the factoring minterm is $\bar{x}_3$ which is a 1st order complemented minterm; the factorised minterms are direct, 1st order direct and complemented minterms with $D = 1$, $d = 2$, $C = 1$.

According to Table 2 line 13 ($D + c$ is odd) the saving of gates, with respect to the general (NAND-NOR) XOR synthesis (cases * and ** are not considered), is $D + 2d - 2 = 3$ and the synthesis of these four factorised minterms needs $D = 1$ NAND gate, $C + 1 = 2$ NOR gates and 1 XOR gate.

The last four terms may be written

$$x_3 \bar{x}_4 \oplus x_2 x_3 x_4 \oplus x_1 x_3 x_4 x_5 \oplus \bar{x}_1 \bar{x}_2 x_3 =$$
$$= x_3 (\bar{x}_4 \oplus x_2 x_4 \oplus x_1 x_4 x_5 \oplus \bar{x}_1 \bar{x}_2)$$

The initial minterms are direct and mixed; the factoring minterm is x_3; the factorised minterms are direct, complemented and 1st order complemented and their number respectively are $D = 2, C = 1$ and $c = 1$. According to Table 2 line 11 ($d = M = 0$) the saving of gates is $C + 2c - 3 = 0$ and the synthesis needs a total of six gates, $D = 2$ NAND gates, $C + 1 = 2$ NOR gates, 1 INV gate and 1 XOR gate.

The general (NAND-NOR) XOR synthesis of the only first four terms needs, according to Table 1 line 8, with $M^* = 3$ and $C = 1$, $M^* = 3^*$ NAND gates and $C + M^{**} = 4^{**}$ NOR gates and the total cost is seven gates; $3^*/$ may reduce to $1/$ and $2\emptyset$; $4^{**}\downarrow$ may reduce to $2\downarrow$ and $1\emptyset$ the two above reductions are not cumulative since some minterms are used for each reduction. Finally, the minimum cost is 3 NAND gates, 2 NOR gates and 1 INV gate, i.e. six gates.

The general (NAND-NOR) XOR synthesis of only the last four terms needs $D + M^* = 2 + 2^* = 4^*$ NAND gates and $M^{**} = 2^{**}$ NOR gates (Table 1, line 6) i.e. 6 gates. $4^*/$ may reduce to $2/$ and $1\emptyset$; the minimum cost is then $2/$, $2\downarrow$, $1\emptyset$, i.e. 5 gates. We shall consider two reduced (NAND-NOR) XOR factorised synthesis. Using the first factorisation only, the predicted cost is: $7 - 3 + 5 + 1 = 10$ gates where 7 is the general cost of the first four terms and 3 the saving of gates, 5 the minimum cost of the last four terms and 1 the XOR output gate. And using both factorisations, we obtain

$$4 + 6 + 1 = 11 \text{ gates}$$

where 4 is the cost of the factorised first four terms and 6 that of the factorised last four terms.

In these two last cases no further saving can be obtained by merging of INV gates since the first factorised form does not need any INV gate. Using the second factorisation only we obtain

$$6^* + 6 + 1 = 13 \text{ gates}$$

where 6^* is the minimum synthesis cost of the first four minterms and 6 the synthesis cost of the factorised last four minterms and 1 the output gate; 6^* reduces to 5 since an INV gate may merge ($\bar{x}_3$ both appears in the unfactorised and factorised part of the NAND-NOR expression) and so finally 12 gates are needed. Hence the lowest synthesis cost obtained in this way is 10 gates and the corresponding expression of f is:

$$f_1 = (x_3 \underset{2}{\downarrow} (x_1 \underset{3}{\oplus} x_2 \oplus (x_2 \underset{4}{\downarrow} x_4 \downarrow x_5) \oplus (x_2/x_4/x_5))) \underset{1}{\oplus}$$
$$(\bar{x}_3 \underset{6}{\downarrow}\underset{7}{} x_4) \oplus (x_2/x_3/x_4) \underset{8}{\oplus} (x_1/x_3/x_4/x_5) \underset{9}{\oplus} (x_1 \underset{10}{\downarrow} x_2 \downarrow \bar{x}_3)$$

When only two-input XOR gates are available, 6 extra XOR gates are required for the unfactorised form whereas 5 or 4 extra XOR gates are required for the factorised forms respectively obtained by one factorisation or by both factorisations.

Factorisation is then much more advantageous and the minimum cost is obtained with f_1 (given above) or f_2 given by

$$f_2 = (x_3 \underset{2}{\downarrow} (x_1 \underset{3}{\oplus} x_2 \oplus (x_2 \underset{4}{\downarrow} x_4 \downarrow x_5) \oplus (x_2/x_4/x_5)) \underset{1}{\oplus}$$
$$(\bar{x}_3 \underset{6}{\downarrow}\underset{7}{} (x_4 \underset{8}{\oplus} (x_2/x_4) \underset{9}{\oplus} (x_1/x_4/x_5) \underset{10}{\oplus} (x_1 \underset{11}{\downarrow} x_2)))$$

for which 11 gates are required.

6. Conclusion

Saving of gates can be obtained when some minterms of a modulo 2 sum of minterms are factorised. General results are tabulated. Technological restrictions are easily taken into account.

References

BANKS, W. and MAJITHIA, J. C. (1973). Design and application of a modified universal logic module, *Proc. IEEE*, Vol. 61, p. 687.

BIVOL, L. G. (1968). Realization of Boolean function by a single sum mod. 2 element, *Autom. and Rem. Contr.* Vol. 6, pp. 959-961.

CSANKY, F. (1969). A new map method for symplifying functions given by exclusive-Or and NAND and inverter operations, *Act. Techn. Electric. Engineer*, Vol. 13, pp. 341-344.

EDWARDS, C. R. (1975). The manipulation of Boolean expressions containing the exclusive-Or operator, *Int. J. Electronics*, Vol. 89, pp. 687-690.

EDWARDS, C. R. and HURST, S. L. (1976). Analysis of universal logic modules, *Int. J. Electronics*, Vol. 41 no. 6, pp. 625-628.

LOTFI, Z. (1977). Thèse de Docteur-Ingénieur, Université de Nancy I.

MIESSLER, M. H. (1972). Use of exclusive-Or gates for Boolean minimization, *Pr. IEEE*, Vol. 119, pp. 1269-1272.

MUKHOPADHYAY, A. and SCHMITZ, G. (1970). Minimization of exclusive-Or and logical equivalence switching circuits, *IEEE Trans. on comp.*, Vol. C19, pp. 132-140.

SCHMOOKLER, M. S. (1969). On mod. 2 sums of products, *IEEE Transactions on computers*, Vol. C18 no. 7, pp. 957-958.

TOSSER, A. (1975). Etude des modes centralisé, distribué, concentré et hybride d'inhibition simple de formes logiques disjonctives de fonctions booléennes matérialisées à l'aide de portes ET-NON et OU-NON, *Automatisme*, XX, pp. 366-390 et 456-470.

TOSSER, A. (1976). Opportunity of inhibition to optimize NAND-NOR networks, *Comput and Electr. Engineer*, Vol. 3, pp. 281-292.

TOSSER, A. et BROCHET, P. (1974). Recherche de la synthèse optimale avec des portes ET-NON et OU-NON de formes disjonctives ou conjonctives de fonctions booléennes à l'aide du symbolisme bulle, *Automatisme*, XIX, pp. 101-116.

TOSSER, A. et LOTFI, Z. (1978). Rapport interne 02 du Laboratoire d'Electronique de l'Université de Nancy I.