

dropping a message is relatively large. As messages pass through the network, some messages will be dropped off. Thus, although the network loading in the switching elements of the first stage is 100 percent, the network loading at later stages decreases gradually due to message dropping. From the previous analysis, we have seen that the lighter the network loading, the more effective the short-circuit switching. Therefore, for small  $n_b$ , the probability that a message can bypass a buffer in short-circuit is high and throughput in short-circuit network is higher than that in message switching. As  $n_b$  increases, less messages are dropped and the network loadings at each stage become closer to 100 percent, which renders the short-circuit switching less effective. Therefore, for large  $n_b$ , the throughputs of the two networks become closer. Since the network contains 32 source PEs and the average transmission time is 10 time units, the limit for the throughput of the network is 3.2 messages per time unit. From Fig. 8, we see that both curves will approach the limit when the number of buffers are larger than 16.

## 6. CONCLUSIONS

From the analytical and simulation results, it is seen that networks with short-circuit switching outperform store-and-forward networks and circuit switching networks, especially in large networks under moderate loading conditions. When network loading is low, short-circuit works like circuit switching and so, delay time is reduced since there is no delay in each stage. When network loading is heavy, short-circuit switching exploits the advantages of store-and-forward networks (i.e., pipeline transmission) and thus increases the throughput.

The simulation presented in this paper is limited to networks of relatively small sizes. However, by extrapolating the simulation results, we can predict that short-circuits are exploited more effectively when the network size is larger. The more the number of stages of the network, the more flexibility exists for establishing partial paths.

The hardware complexity of the switching elements used in short-circuit switching networks is comparable to those used in message switching networks [8]. Both use four queues of buffers in each switching element. The only additional hardware needed to implement short-circuits is four multiplexers, four demultiplexers, and some logic circuits to control these multiplexers and demultiplexers.

## REFERENCES

1. N. J. Davis IV and H. J. Siegel, Performance studies of multiple-packet multistage cube networks and comparison to circuit switching, *1986 International Conference on Parallel Processing*, pp. 108–114 (1986).
2. K. Hwang and F. Briggs, *Computer Architecture and parallel processing*, McGraw-Hill Book Company, 1984.
3. U. V. Premkumar and R. N. Kapur, M. Malek, G. J. Lipovski, and P. Horne, Design and implementation of the banyan interconnection network in TRAC, *AFIPS 1980 National Computer Conference*, pp. 643–653 (1980).
4. L. N. Bhuyan, Q. Yang and D. P. Agrawal, Performance of multiprocessor interconnection networks. *Computer* 22, (2), 25–37 (1989).
5. A. Gottlieb, R. Grishman, C. Kruskal, K. McAuliffe, L. Rudolph and M. Snir, The NYU Ultracomputer—Designing an MIMD Shared Memory Parallel Computer, *IEEE Trans. on Computers* C-32, (2), 175–189 (1983).
6. D. Gajski, D. Kuck, D. Lawrie and A. Sameh, Cedar—A large scale multiprocessor, *Proc. of the 1983 International Conference on Parallel Processing*, pp. 524–529.
7. G. F. Pfister and V. A. Norton, 'Hot Spot' Contention and Combining in Multistage Interconnection Networks, *Proc. of the 1985 International Conference on Parallel Processing*, pp. 790–797.
8. E. D. Brooks, Performance of the Butterfly Processor-Memory Interconnection in a Vector Environment, *Proc. of the 1985 International Conference on Parallel Processing*, pp. 21–24.
9. C. P. Kruskal and M. Snir, The performance of multistage interconnection networks for multiprocessors, *IEEE Trans. on Computers*, C-32, (12), 1091–1098 (1983).

## Announcement

12–14 SEPTEMBER 1990

GUILDFORD, UK

### International Professional Communication Conference

Sponsored by: The IEEE Professional Communication Society, United Kingdom and Republic of Ireland Section, Region Eight

### Theme—Communication Across the Sea: North American and European Practices

Main topics include, but are not limited to:

- Technical Communication: Part of the Engineer's Job or a Job for a Specialist?

- Proposal Preparation: United States and European Approaches.
- Is There both a British and an American English?
- Trends in International Standards for Engineering Communication.
- The Paperless Office: Is it Possible, and How?
- Automated Text Processing: Desktop Publishing Grammar and Syntax Assistance.
- Modern Approaches to Machine Translation.
- Preparing Camera-Ready Mathematical Copy.
- Computer Generated Graphics.

- The Skills of Technical Communication: When and How are They Acquired?
- Submitting Manuscripts to Technical Journals.
- Explaining Science and Engineering to the Lay Public.
- The Art of Criticism.
- Why do Mathematicians Find it Difficult to Communicate With Engineers?

*Inquiries should be sent to the IEEE/IPCC-90 Conference Chairman:*

John B. Moffett—The Johns Hopkins University Applied Physics Laboratory, Johns Hopkins Road, Laurel, MD USA 20707. Tel: (301) 953 5000 x8260. Fax: (301) 953 1093.