

# Capsule Reviews

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The Capsule Reviews are intended to provide a short succinct review of each paper in the issue in order to bring it to a wider readership. The Capsule Reviews were compiled by Fairouz Kamareddine. Professor Kamareddine is an Associate Editor of *The Computer Journal* and is based in the Department of Mathematical and Computer Sciences at Heriot-Watt University, Edinburgh, UK.

## Scalable Federated Broker Management for Selection of Web Services. MOHAMED ADEL SERHANI, ABDELGHANI BENHARREF, ELARBI BADIDI AND SALAH BOUKTIF

Although several research initiatives have investigated the issue of Web Services management, key Quality of Web Services (QoWS) characteristics such as scalability, trust, reliability and support of a range of QoWS driven operations are still lacking. This paper aims to tackle these issues and proposes a federated broker-based architecture for selecting, monitoring and certifying QoS-aware Web Services. First, a formulation of the selection problem solved by the federation of brokers is given and the backgrounds for quality of services properties and the concept of federation are introduced. Then, related works and their drawbacks are covered and the objectives for a better support for QoWS during different phases of interactions are presented. The authors propose an architecture and a framework that meets those objectives. This includes the broker components/interfaces and the brokers' federation management. The authors explain how the federation supports the operations of: certification and monitoring of Web Services and brokers, and selection of Web Services. After an evaluation of the communication and monitoring overhead, an illustrative example of federation of brokers for selection of travel package Web Services is given. The feasibility of the proposed architecture is demonstrated through a proof of concept prototype where a series of experiments are conducted to evaluate the QoWS-aware Web Service selection schemes. In particular, selection capabilities, scalability and monitoring overhead are evaluated and the results are analyzed. Finally, the authors discuss the internal, external and construct threats to the validity of their experiments.

## Node-to-Set Disjoint-Path Routing in Hierarchical Cubic Networks. ANTOINE BOSSARD AND KEIICHI KANEKO

This paper focuses on hierarchical cubic networks (HCNs) which have almost half as many edges as a comparable hypercube. Given a source node and a set of destination

nodes, the node-to-set disjoint-path routing problem is about finding node-disjoint paths between the source node and every destination node. This paper proposes a node-to-set disjoint-path routing algorithm HCN-N2S inside an HCN. After an introduction to the needed preliminaries, the proposed node-to-set disjoint-path routing algorithm HCN-N2S in a hierarchical cubic network  $HCN(n)$  is given where a hierarchical cubic network  $HCN(n)$  has a connectivity of  $n + 1$ . The correctness and time complexity of special HCN-N2Ss and an upper bound for the maximum path length are given.

## High-Performance IP Lookup Engine with Compact Clustered Trie Search. OÜGUZHAN ERDEM AND CUNEYT F. BAZLAMACCI

In IP lookup, a router finds the address of a next-hop router or egress port through which a packet should be sent. Most hardware-based packet-forwarding engines for network routers fall into two main categories: ternary content addressable memory (TCAM)-based and dynamic/static random access memory (DRAM/SRAM)-based solutions. This paper notes that SRAM has better density, power consumption and speed characteristics compared with TCAM and proposes a novel dual port SRAM-based four-side IP lookup architecture, which is built upon a systolic array-like architecture for fast IP lookup (SAFIL). The proposed four-side architecture employing dual input/output SRAMs and compact clustered binary trie (CCT) is denoted by SAFILD-CCT. After an overview of SRAM-based pipeline architectures for fast IP lookup, and of Systolic array architecture for fast IP lookup, the authors present their proposal of SAFIL with dual-port SRAMs and four-side input using CCT. Algorithms for the construction of a CCT and for IP-lookup are given and basic designs for processing elements, selector units, congestion control and cache use are detailed. Simulations using real-life backbone IP packet traces were conducted and it was established that use of SAFILD-CCT brings a number of advantages. A comparison with other architectures is also given.