

An extension of block design methods and an application in the construction of redundant fault reducing circuits for computers

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In a balanced block design one's aim is to arrange a number of objects in a number of blocks according to certain rules. There is a certain class of design in which the blocks can be conceived as operating upon the objects to produce new objects which, in turn, may enter a further design. In this case not only does the block operator have to be taken into account, but arrangements of objects and blocks, normally regarded as indistinct in a block design, can have an important effect on the properties of the design. These ideas are applied to the design of simple fault detecting and correcting computer redundancy circuits. Here the criterion of goodness for design is not just the fault reducing properties obtained by a single pass of information through the circuit, but the further effect of information encountering a sequence of such circuits.

To detect, and more ambitiously to correct, faults which occur in the generation and transmission of information, it is necessary to generate and transmit extra redundant information. This may be achieved either by carrying redundant information bits with the information word (parity bits), or by parallel transmission of the information words in a "bundle" of channels, and comparison at their destination. The latter method would appear wasteful in the amount of redundancy which it demands but has been studied by Pierce (Pierce, 1962) and others, particularly as it is used in biological mechanisms. However, the redundant equipment required is very simple, and the striking success which can be obtained with simple devices suggests that their use in computer circuitry would be effective and economic.

This paper uses the block design method for the study of redundancy circuits based on majority vote takers. A computer has been used in a systematic study of these extended block design conditions. A very simple redundancy circuit with good fault reducing properties is described.

Though the terms "error detection" and "error correction" are commonly used, we prefer to use the word "fault" in this paper and to reserve "error" for the numerical errors studied in Numerical Analysis.

1. Introduction

1.1. Block design theory

We use the block design notation of Hall (Hall, 1962) and summarize here those concepts which we shall use.

In a balanced block design we consider v objects contained in b blocks so that

- (i) each block contains k distinct objects,
- (ii) each object occurs in r distinct blocks,
- (iii) each pair of objects occurs together in exactly λ blocks.

Then the five parameters v , b , k , r , and λ satisfy two simple relations:

$$bk = vr \quad (1.1)$$

$$r(k - 1) = \lambda(v - 1). \quad (1.2)$$

There are further conditions imposed upon the parameters in order that a design exists. A sufficient set of conditions is not known, but necessary conditions have been given by Chowla and Ryser (Chowla and Ryser, 1950).

In a so-called *symmetric design* $b = v$. Then from (1.1) $k = r$, and (1.2) reduces to

$$k(k - 1) = \lambda(v - 1). \quad (1.3)$$

Such a design is called symmetric because in it we can say, in addition to (iii), that

- (iv) any pair of blocks share exactly λ objects.

The roles of block and object become dual in a symmetric design, and interchanging them gives another block design having the same parameters but not necessarily isomorphic to the first.

The *incidence matrix* of a block design is, in general, a $b \times v$ matrix of ones and zeros where the elements a_{ij} are such that

$$a_{ij} = 1 \text{ if object } a_i \in \text{block } B_j$$

$$\begin{aligned} \text{otherwise} \quad a_{ij} &= 0 \\ \text{and} \quad i &= 1, 2, \dots, v \\ j &= 1, 2, \dots, b. \end{aligned}$$

1.2. Application

In our application we regard as the objects of a block design the v lines of an input bundle carrying v simultaneous copies of binary information. The blocks are b majority votetakers each with k inputs and one output. In general there are, therefore, b lines in an output bundle. To examine the passage of information through a series of such circuits it is convenient to have informa-

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tion bundles containing a constant number of lines. Our designs will thus be symmetric designs with $b = v$.

In our redundancy circuits we can regard the incidence matrix of the design as a *maze matrix* which describes the interconnections of the lines of the input bundle to the inputs of the votetakers. For symmetric designs the maze matrix is square.

As an example, consider the fault correcting device of Fig. 1. $v = 7$ is the number of lines in the input bundle. $b = 7$ is the number of lines in the output bundle. $k = 3$ describes the number of inputs possessed by each votetaker. In this design the maze which interconnects the input lines with the votetakers is such that any two votetakers only have one common input line, and any two input lines only go to one votetaker. This condition is described by the parameter $\lambda = 1$. With the definition of Section 1.1 it can be seen further that the maze matrix (Matrix 1) given in Section 2.2 completely describes these interconnections.

In examining the design properties for circuits which will be encountered successively by transmitted information, the dual designs contained within a symmetric design have a special significance, and associated with this the product matrix $[a_{ij}]^2$ becomes important.

1.3. Majority votetaker properties

The simplest majority votetaker is a 3-input gate for which the transformation of inputs a, b, c , each regarded as a train of binary digits, is given in terms of *and* (\wedge) and *or* (\vee) operators as follows:

$$a \oplus b \oplus c =$$

$$(a \wedge b \wedge c) \vee (a \wedge b \wedge \bar{c}) \vee (a \wedge \bar{b} \wedge c) \vee (\bar{a} \wedge b \wedge c)$$

where \oplus indicates the votetaker operator.

The property extends simply, in general, to k input votetakers.

In terms of hardware then, a 3-input votetaker consists of four 3-input and-gates and one 4-input or-gate. This is effectively of the order of 16 diodes and 5 resistors.

It is interesting to note, in passing, that, in computer simulation of votetakers, the *or* operators can be replaced by ordinary binary additions. This is only possible because of the particular form of the contents of the brackets.

2. Criteria of goodness for a fault reducing redundancy circuit

We can distinguish two criteria for judging the success of a fault reducing circuit.

1. We can examine the success of a circuit in reducing the number of faults on a single pass of information.
2. We can examine the fault reducing properties when a circuit is presented with successive passes of information (or when information is presented to a sequence of similar circuits).

In both cases the fault reducing properties depend on the transformation properties of the individual vote-

takers, and on their combined effect which in turn depends on the design.

2.1. Reduction of faults in a single pass

Single votetaker

If R is the number of faults presented to a single k -input votetaker then, of course, $0 \leq R \leq k$.

For such a votetaker when $0 \leq R < \frac{1}{2}(k + 1)$ the R faults will be cured instantly; when $\frac{1}{2}(k + 1) \leq R \leq k$ the R faults will propagate as a fault on the output line.

Combined circuit

For a number of k -input votetakers interconnected to an input bundle by a maze it is still true that $R < \frac{1}{2}(k + 1)$ simultaneous faults will be cured. By imposing a restriction on the parameter of the design we can further improve the fault reducing properties of the circuit as follows. If $\lambda < \frac{1}{2}(k + 1)$ then

- (a) Any R simultaneous faults with $R = \frac{1}{2}(k + 1)$ will, at most, propagate as a single fault.
- (b) There are ${}_v C_k$ possible R simultaneous faults with $R = k$. Of these v possibilities reduce to single faults.

PROOF:

- (a) This follows since the R faults, if presented to a single votetaker will propagate as a fault, but at most λ (which is $< \frac{1}{2}(k + 1)$) of the faults will arrive at any other votetaker and will be cured.
- (b) Each of the sets of k simultaneous faults which reduce to a single fault consist of those k faults presented to a specific votetaker (of which there are v). Then the faults of a particular set propagate on that votetaker, but the restriction on λ ensures that there is no propagation on any other.

Thus acceptable fault reducing properties for a single pass of information are obtained by adding the condition

$$\lambda < \frac{1}{2}(k + 1)$$

to the restrictions (1.1), (1.2), (1.3), and the conditions of Chowla and Ryser for the parameters v, k, λ .

We list the possible parameters for designs based on k -input votetakers for the first few values of k in Table 1.

Table 1
Possible design parameters for simple redundancy circuits for first few values of k

k	v	λ
3	7	1
5	21	1
5	11	2
7	15	3
9	73	1
11	57	2

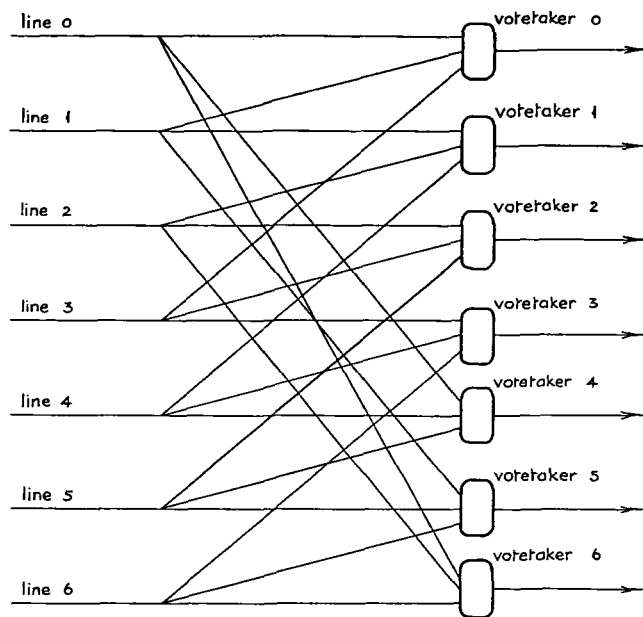


Fig. 1.—A simple fault reducing redundant circuit

2.2. A specific example

Most of our attention has been centred on the simplest case of a balanced block design with parameters $k = 3$, $v = 7$, $\lambda = 1$. (Such a block design has an interesting geometrical analogy. It is equivalent to a finite projective plane of order 6.) There are a number of possible designs with these parameters, two of which possess automorphisms.

An *automorphic* design is one having an incidence matrix which is circulant in form. That is, each row is equivalent to the row above cyclically right shifted one place. This symmetry gives the designs interesting group-theoretical properties. In particular an automorphic design is completely described by one row of its incidence matrix. Matrix 1, then, is completely described by the position numbers 0, 1, 3 of the non-zero elements of the first row. Hall calls these numbers 0, 1, 3 (mod 7) the *difference set* because any possible position number 0 (1) 6 is expressible as the difference, modulus 7, of a pair of these. In this case, for example,

$$\begin{aligned} 0 &= 0 - 0 & 2 &= 3 - 1 & 4 &= 0 - 3 & 6 &= 0 - 1 \\ 1 &= 1 - 0 & 3 &= 3 - 0 & 5 &= 1 - 3. \end{aligned}$$

As mentioned later, another automorphic design with parameters $k = 3$, $v = 7$, $\lambda = 1$ has a difference set 0, 1, 5 (mod 7).

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{Matrix 1}$$

The specific redundant circuit design corresponding to this matrix is shown in Fig. 1.

With parameters $k = 3$, $v = 7$, $\lambda = 1$:

all single faults are cured immediately,
all double faults (there are ${}^7C_2 = 21$) reduce to single faults,
7 triple faults reduce to single faults.

The remaining $35 - 7 = 28$ triple faults are propagated as triple faults. The detailed analysis of propagation of triple faults from input lines to output lines for the above design is as follows:

012 → 016	123 → 012	345 → 234	
013 0	124 1	346 3	
014 014	125 125	*356 235	
*015 045	*126 156	456 345	
016 056	*134 013		
*023 026	135 025		
024 146	136 035	See next Section	
025 246	145 145	for the	
026 6	146 135	significance	
034 034	156 5	of the	
035 024	234 123	transformations	
036 036	235 2	marked*.	
045 4	236 236		
*046 346	*245 124		
056 456	246 136		
	256 256		

2.3. Reduction of faults in successive passes

In a certain class of block designs, of which our fault reducing circuits are an example, one can regard the blocks as operating upon the objects they contain to produce new objects. These in turn may be regarded as objects in a further block design. In determining the value of a particular design which is subjected to repeated inclusions of objects being transformed in this way, it is important to follow properties of the original objects through their several transformations. The product of the incidence matrix with itself helps considerably in this study. In $[a_{ij}]^2$ the j th element of the i th column tells how many times objects in the j th block of the second design claim descent from the i th object in the first design.

In the design of the last Section, 7 triple faults reduced at once to single faults. It will be seen that 7 more, marked *, though transforming into further triple faults, will reduce to single faults after a second encounter with a similar circuit. All other triple faults, however, form cycles among themselves and never reduce after successive transformations. In particular some triple faults, like 014, simply transform repeatedly into themselves. We put the triple fault reducing properties of the design into a tabular form in Table 2. The other block design with parameters $k = 3$, $v = 7$, $\lambda = 1$, possessing an automorphism has a difference set 0, 1, 5 (mod 7) and similar properties to the above.

Table 2

Fault reducing transformation table corresponding to Matrix 1

No. of transformations	1	2
No. of triple faults reduced	7	7

Now the mere ordering of blocks in the design can have a marked effect on the successful fault reducing properties. The following maze matrix is obtained from that of the last section by permutation of rows only:

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \end{bmatrix} \quad \text{Matrix 2}$$

The triple fault reducing properties are given in Table 3, and now only 10 triple faults do not reduce.

Consider the properties of $[a_{ij}]^2$ for this design.

$$[a_{ij}]^2 = \begin{bmatrix} 2 & 1 & 2 & 2 & 0 & 1 & 1 \\ 2 & 0 & 1 & 1 & 2 & 1 & 2 \\ 1 & 2 & 0 & 2 & 1 & 1 & 2 \\ 2 & 2 & 1 & 1 & 2 & 1 & 0 \\ 0 & 1 & 2 & 2 & 2 & 1 & 1 \\ 1 & 2 & 2 & 0 & 1 & 1 & 2 \\ 1 & 1 & 1 & 1 & 1 & 3 & 1 \end{bmatrix}.$$

It is intuitively clear that the greatest number of reductions of triple faults will result from the most uniform distribution of input bundle lines among the votetakers, subject to the restrictions imposed on the design parameters already discussed. The presence of the 3 in the last row of the matrix, in this example, shows the lack of uniformity and prevents the 7th votetaker of the second set from reducing a triple fault.

We endeavour to achieve this uniformity by arranging the scalar product of any row and column of the maze matrix to be, at most, 2. Now the rows of the matrix describe the arrangement of objects in blocks, and the columns likewise for the dual design. We can achieve uniformity with greatest element 2 by arranging the dual designs to be the two automorphic designs 0, 1, 3 (mod 7) and 0, 1, 5 (mod 7). A maze matrix with this property is

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \end{bmatrix} \quad \begin{array}{l} \text{Matrix 3} \\ \text{in which row zero} \\ \text{and column 3 are} \\ \text{the defining} \\ \text{difference sets.} \end{array}$$

The fault reducing properties shown in Table 4 show a remarkable improvement. There is now only one non-reducing fault $146 \rightleftharpoons 146$.

Table 3

Fault reducing transformation table corresponding to Matrix 2

No. of transformations	1	2	3	4	5	6	7
No. of triple faults reduced	7	6	3	3	3	2	1

Table 4

Fault reducing transformation table corresponding to Matrix 3

No. of transformations	1	2	3	4	5	6
No. of triple faults reduced	7	7	6	6	5	3

In the next Section we describe a computer algorithm for the construction of these transformation tables in a systematic search through possible block designs, though the design above proves to be one of the best possible.

We see then that in this extension of block design the criterion for goodness of design must depend on the transformations which blocks perform upon the objects, and the purpose to which the design is put. In turn the restrictions upon the design to achieve these ends must depend on the same considerations. However, the powers of the incidence matrix are important since the elements of these matrices describe the effect of properties associated with the original objects on successive designs.

3. A triple fault reduction analysis algorithm

As we have seen, seven triple faults reduce at once to single faults. We can calculate back to the triple fault which reduces to one of these seven and hence reduces to a single fault after two passes. This we do as follows:

Suppose x, y, z describes one of the reducing triple faults. We examine rows x, y and z of the maze matrix and find that they share in pairs elements in positions x^1, y^1 and z^1 . Then x^1, y^1, z^1 is the triple fault which reduces to x, y, z . Continuing in this way we ultimately find that examination of rows $x^{(n)}, y^{(n)}, z^{(n)}$, reveals that all share elements in only one column. This is a row of the dual design and no earlier triple fault is transformed into $x^{(n)}, y^{(n)}, z^{(n)}$.

As an example it can be verified that for the block design defined by Matrix 2 we obtain the following chains:

023 \rightarrow 013 \rightarrow 0
046 \rightarrow 235 \rightarrow 1
136 \rightarrow 045 \rightarrow 2
015 \rightarrow 014 \rightarrow 236 \rightarrow 135 \rightarrow 014 \rightarrow 026 \rightarrow 3
256 \rightarrow 234 \rightarrow 056 \rightarrow 234 \rightarrow 156 \rightarrow 4
345 \rightarrow 125 \rightarrow 146 \rightarrow 456 \rightarrow 245 \rightarrow 126 \rightarrow 346 \rightarrow 5
124 \rightarrow 6.

Hence we start with the triple given in each row and work back through the chain counting how many triples transform into each other and finally reduce. In the

example the set of numbers thus obtained for rows 0, 1, . . . 6 is 2, 2, 2, 6, 5, 7, 1. The i th element in the transformation table is then obtained by evaluating how many numbers of this set are $\geq i$ where $i = 1, 2, \dots$

This gives the transformation Table 3.

This algorithm has been built into a systematic generation of rows of maze matrices satisfying the necessary conditions and programmed for the Stantec Computing System at the Institute of Technology at Bradford. In this way a comprehensive search for the best possible 7th-order maze matrix to be used in association with 3-input votetakers has been made.

Although the automorphic designs with $k = 3$, $\lambda = 1$ are easy to describe, their incidence matrices being circulant in form, there are designs for which this simple structure does not hold. For example, we may have the design with incidence matrix

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix} \quad \text{Matrix 4}$$

These designs were included in the search but they revealed no essential difference with regard to their successive fault reduction properties from the automorphic designs.

It turns out that there are a number of possible matrices which will reduce all triple faults by applying sufficient transformations. The reduction for these matrices is given in Table 5.

Table 5

Fault reducing transformation table for designs in which all triple faults reduce

No. of transformations	1	2	3	4	5	6	7	8	9	10
No. of triple faults reduced	7	7	6	3	2	2	2	1	1	1

No matrices were found which could reduce all faults in few transformations, and the best matrices might still be regarded as those having transformation Table 4, in

spite of the fact that one triple fault escapes reduction altogether. One such design was given explicitly by Matrix 3.

4. Conclusions and suggestion for further study

It appears fruitful in some applications to regard a block design as an operator which transforms its objects into a new set of objects. In subjecting these objects to successive block design transformations, restrictions on the design can sometimes improve its properties.

There is no reason why we should not investigate the effect of *unbalanced* designs in applications such as the one we have described. If, for example, we extend the first automorphic design of Section 2.2 with parameters $k = 3$, $v = 7$, $\lambda = 1$ to have $v = 8$, we might consider the design with incidence matrix

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}.$$

This design is unbalanced, for no longer do two blocks contain a constant number λ of objects in common or are two objects contained in a constant number of blocks. There appears to be little or no development of the theory of unbalanced block design, though such designs may, perhaps, have superior properties in the case of our successive transformation designs.

The simple redundancy circuits described have been used primarily to illustrate the concept of successive transformation designs. More sophisticated circuit designs employing weighted votetakers and combined votetakers and logic gates have been described by Pierce in which the amount of redundancy required can be reduced. The extreme simplicity of circuitry demanded by our basic circuits, and the very good fault reducing properties of some designs involving only seven line bundles suggests, however, that such circuits might be worth employing in their own right.

References

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